REMARKS

I. Present Status of the Application

The specification is objected to because incorrect reference signs are found. The Office Action rejected claims 1, 3-6, 8-13 under 35 U.S.C. § 103(a) as being unpatentable over AAPA (applicant admitted prior art) in view of Patterson et al. (US 5,080,958).

Upon entry of the amendments in this response, the incorrect reference signs in paragraph [0003] are corrected. In addition, claim 6 is amended and claims 1, 3-5, 7-10 and 13 are canceled without prejudice. After entry of the foregoing amendments, claims 6, 11-12 remain pending in the present application, and reconsideration of those claims is respectfully requested.

II. Response to Rejections under 35 U.S.C. § 103(a)

Applicants respectfully traverse the rejection of claims 6, 11-12 under 103(a) as being unpatentable over AAPA in view of Patterson et al. (US 5,080,958) because a prima facie case of obviousness has not been established by the Office Action.

To establish a prima facie case of obviousness under 35 U.S.C. 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element in the claims. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three

requirements must " be found in the prior art, and not be based on applicant's disclosure." See M.P.E.P. 2143, 8th ed., February 2003.

The present invention is in general related a chip package structure as claim 6 recites:

Claim 6. A chip package structure, comprising:
a hybrid integrated circuit (IC) carrier having a first surface and a second surface, wherein the hybrid IC carrier at least having:
a plurality of patterned conductive layers stacked over each other, wherein the patterned conductive layer closest to the first surface furthermore has a plurality of bonding pads thereon;
a plurality of dielectric layers respectively sandwiched between a pair of neighboring patterned conductive layers, ***wherein at least one of the dielectric layers is a ceramic dielectric layer with one ceramic dielectric layer positioned with all the remaining dielectric layers on one side thereof***, and at least one of the remaining dielectric layers is an organic dielectric layer; and
a plurality of vias passing through at least the dielectric core layer for connecting at least two of the patterned conductive layers electrically; and
a chip attached to the first surface of the hybrid IC carrier and connected electrically to the hybrid IC carrier via the bonding pads, ***wherein the ceramic dielectric layer is attached to the chip on the first surface of the hybrid IC carrier.***

Patterson fails to teach or suggest that one ceramic dielectric layer is positioned with all the remaining dielectric layers on one side thereof, and the ceramic dielectric layer is attached to the chip on the first surface of the hybrid IC carrier. In Patterson's reference, the interconnect includes a ceramic substrate 1 having conductive patterns 2 thereon, a dielectric layer 3, adhesive layers 6, 8, an organic film 7 and a metal foil layer 9. In particular, a discrete component 13 having leads 12 is soldered onto the pattern (metal foil layer) 9. Therefore, the discrete component 13 disclosed by Patterson is soldered onto the metal foil layer 9 but not attached to the ceramic layer 1. In addition, the feature of "one ceramic dielectric layer is positioned with

all the remaining dielectric layers on one side thereof, and the ceramic dielectric layer is attached to the chip on the first surface of the hybrid IC carrier" is not disclosed in AAPA.

Thus, Patterson's structure is rather different from the chip package structure of this invention, and one of ordinary skills in the art would not have been motivated to combine Patterson's teaching with the structure disclosed in AAPA. Even if a combination were made, the resulting structure would have been different from that of the claimed invention.

Therefore, the amended claims of this invention are not rendered obvious over the prior art references. Accordingly, Applicants respectfully submit that the grounds of rejection have been addressed and the rejection has been overcome. Reconsideration and withdrawal of the rejection are respectfully requested.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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